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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,959	12/10/2003	David L. Collins	200300473-1	6774

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EXAMINER

VIDWAN, JASJIT S

ART UNIT PAPER NUMBER

2182

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/731,959	COLLINS, DAVID L.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 June 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>12/10/2003</u>  | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 101***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claim 42 is rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well-established utility.

Claim 42 claims a microcontroller programmed to avoid conflicts with other devices and to reduce resource consumption. The claim as recited lacks specific and substantial asserted utility because the specification disclosed does not disclose means for avoiding conflicts and reducing resource consumption within itself because when claims depend on a recited property, a fact situation comparable to Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) is possible, where the claim covers every conceivable structure (means) for achieving the stated property while the specification discloses at most only those known to the inventor.

Claim 42 also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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3. Claim 42 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a computer system that comprises a microcontroller that functions as a south bridge, does not reasonably provide enablement for a single microprocessor to avoid conflict and reduce power consumption. The specification at best discloses a microcontroller having various interfaces in conjunction with the storage device to control the communication with the peripheral devices. The claim as is does not enable any person skilled in the art to make and use the invention commensurate in scope with these claims. A single means claim which covers every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor for the purpose of how to make a microcontroller being programmed to avoid conflicts with other devices and to reduce resource consumption.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 1 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 23 reads as microcontroller having a "communication interface that is adapted to allow communication between the communication interface and the peripheral device." It is unclear how the communication interface can allow communication between 'itself and the peripheral device. It seems more appropriate for the communication interface to allow communication between System bus and device interfaces to make it more in line with the Claims 12 and 31. For the purpose of timely examination, Examiner will construe 'communication interface' as claimed and more clearly recited in Claim 31 as an interface used by the computer system to communicate with the peripheral devices through device interfaces.

6. Claim 42 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear to the Examiner as previously addressed as to how the Applicant

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intents to program the microcontroller to avoid conflicts with other devices and to reduce resource consumption.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 6, 10, 11, 12, 13, 17, 21, 22, 23, 24, 26, 30, 31, 32, 36, 40, 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Houlberg et al U.S. Patent 5,887,198 [herein after Houlberg].

3. As per Claims 1, 12, 23, 31 and 42 Houlberg teaches in figures 1-3 a system for controlling peripheral devices in a computer system, the system for controlling peripheral devices [Fig. 1, Element 24 and 26] comprising:

(a) Microcontroller [Fig. 2, Element 10, “Embedded PC server”] that provides a plurality of device interfaces [Fig. 3, Element 40 & 42, “PCMCIA Interface”] each of the device interfaces being adapted to support a peripheral device [Fig. 3, Elements 44-50], and a communication interface that is adapted to allow communication with the peripheral devices via the plurality of device interfaces [Fig. 1, Element 28, “Ethernet Interface” – Ethernet interface provides the Client, Fig. 2, element 12, communication to the peripheral devices, Fig. 1, Elements 24, 26, through device interface Fig. 1, Element 22]

(b) Device that stores programming instructions [Fig. 2, Element 16] to initialize the microcontroller separately from the initialization of the computer system [Col. 3, Lines 37-42 – Computer system (Fig. 2, Element 12) is a separate PC that is initialized independently to the Embedded PC FTP serve, Fig. 2, Element 10] The controller 10 enables communication of peripheral device and computer and therefore avoids conflict and reduces resource consumption.

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4. **As per Claim 2, 13, 24 and 32**, Houlberg teaches a system comprising an auxiliary power source **[Fig. 1, Element 34]** that supplies power to the microcontroller separately from a main power supply that supplies power to the system **[Col. 3, Lines 31-35]**.
5. **As per Claim 6, 17, 26 and 36**, Houlberg teaches a system wherein the means for interfacing provides power management functionality for at least one of the peripheral devices **[Col. 3, Lines 31-45, Controller distributes appropriate power to peripheral device from power source]**.
6. **As per Claims 10, 21, 30 and 40**, Houlberg teaches a system wherein the microcontroller provides emulation for at least one of the peripheral devices **[Col. 4, Lines 16-31 – emulating peripheral devices through PCMCIA interface]**.
7. **As per Claims 11, 22 and 41**, Houlberg teaches a system comprising of a local memory associated with the microcontroller **[Fig. 2, Elements 18, 20]**.
8. Claims 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 17, 18, 19, 20, 21, 22, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 36, 37, 38, 39, 40, 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Wunderlich U.S. Patent 6,122,679 **[herein after Wunderlich]**.
9. **As per Claims 1, 12, 23 and 31**, Wunderlich teaches a system for controlling peripheral devices in a computer system, the system for controlling peripheral devices **[Fig. 1, Element 85, 90, 92]** comprising:
- (a) Microcontroller **[Fig. 1, Element 10]** that provides a plurality of device interfaces **[Fig. 2 Element 130, 140, 145, 135, 155, 170]** each of the device interfaces being adapted to support a peripheral device **[Fig. 2, “USB Port, IDE”]**, and a communication interface that is adapted to allow communication with the peripheral devices via the plurality of device interfaces **[Fig. 2, Element 185, “PCI Target Interface”]**
  - (b) Device that stores programming instructions to initialize the microcontroller separately from the initialization of the computer system **[Fig. 1, Element 91]**

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10. **As per Claim 42**, Wunderlich teaches a computer system that comprises a microcontroller **[Fig. 1, Element 10]** those functions as a south bridge **[Fig. 1, Element 100]**. As best interpreted by the Examiner, communication interface that allows communication with the peripheral device via plurality of device interfaces will avoid conflict and reduce resources **[Fig. 2, Element 185, "PCI Target Interface".]**

11. **As per Claim 2, 13, 24 and 32**, Wunderlich teaches a system comprising an auxiliary power source that supplies power to the microcontroller separately from a main power supply that supplies power to the system **[Fig. 2, Element 165, "ACPI/power management logic"]**.

12. **As per Claim 3, 14, and 33** Wunderlich teaches a system wherein the communication interface comprises a Peripheral Component Interface ("PCI") interface **[Fig. 2, Element 185]**.

13. **As per Claim 6, 17, 26 and 36**, Wunderlich teaches a system wherein the means for interfacing provides power management functionality for at least one of the peripheral devices **[Col. 10, Lines 45-51]**.

14. **As per Claims 7, 18, 27 and 37**, Wunderlich teaches a system wherein at least one of the peripheral devices is a Super I/O controller **[Col. 6, Lines 43-46]**.

15. **As per Claims 8, 19, 28 and 38**, Wunderlich as modified by Wunderlich above teaches a system wherein the means for interfacing is defined to be a subtractive decode agent for the computer system **[Col. 8, Lines 55-60]**.

16. **As per Claim 9, 20, 29 and 39**, Wunderlich teaches a system comprising reset logic that resets the system under control of the microcontroller **[Col. 9, Lines 19-25]**.

17. **As per Claims 10, 21, 30 and 40**, Wunderlich teaches a system wherein the microcontroller provides emulation for at least one of the peripheral devices **[Col. 7, Lines 22-30, – emulating peripheral devices through PCMCIA interface]**.

18. **As per Claims 11, 22 and 41**, Wunderlich teaches a system comprising of a local memory associated with the microcontroller **[Fig. 1, Elements 75]**.

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19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. Claims 3, 4, 5, 7, 8, 9, 14, 15, 16, 18, 19, 20, 27, 28, 29, 33, 34, 35, 37, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houlberg and further in view of Wunderlich, U.S. Patent No: 6,122,679 [**herein after Wunderlich**].

21. **As per Claims 3, 4, 5, 14, 15, 16, 33, 34 and 35**, Houlberg teaches the limitations of Claims 1, 12, 23 and 31, as well as communication interfaces that include SCSI, MIL-STD-1153 and Ethernet interface. Houlberg however fails to teach communication interfaces where the interface specifically is one of either Peripheral Component Interface ("PCI") interface, Extended Peripheral Component Interface ("PCI-X") interface or Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface. Wunderlich teaches the limitation of having the communication interface as being Peripheral Component Interface ("PCI") interface [**Figure. 2, Element 185**].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to use PCI interface to take advantage of PCI data transfer speeds. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings in order to take advantage of PCI data transfer speeds. It would have been further obvious to one of ordinary skill in the art at the time of Applicant's invention to select from any one of the above interfaces as deemed suitable in order to provide communication between computer system and various commercially available peripheral device to allow more flexibility for types of I/O devices a system handles. This is further demonstrated by Applicant's various embodiments of interfaces as claimed absent persuasive evidence that a particular type of interface element is significant.



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22. **As per Claims 7, 18, 27 and 37**, Houlberg as modified by Wunderlich above teaches a system wherein at least one of the peripheral devices is a Super I/O controller **[see Wunderlich, Col. 6, Lines 43-46]**.

23. **As per Claims 8, 19, 28 and 38**, Houlberg as modified by Wunderlich above teaches a system wherein the means for interfacing is defined to be a subtractive decode agent for the computer system **[Col. 8, Lines 55-60]**.

24. **As per Claim 9, 20, 29 and 39**, Houlberg as modified by Wunderlich above teaches a system comprising reset logic that resets the system under control of the microcontroller **[Col. 9, Lines 19-25]**.

25. Claims 4, 5, 15, 16, 25, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wunderlich, U.S. Patent No: 6,122,679 **[herein after Wunderlich]**.

26. **As per claims 4, 5, 15, 16, 25, 34 and 35**, Wunderlich teaches the limitations of Claim 1, 12, 23 and 31 in addition to a PCI interface **[Fig. 2, Element 185]**. Wunderlich fails to teach a system wherein the communication interface is also PCI-X interface and SAPIC.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to select from any one of the above (PCI-X and SAPIC) interfaces as deemed suitable in order to provide communication between computer system and various commercially available peripheral device to allow more flexibility for types of I/O devices a system handles. This is further demonstrated by Applicant's various embodiments of interfaces as claimed absent persuasive evidence that a particular type of interface element is significant.

### ***Conclusion***

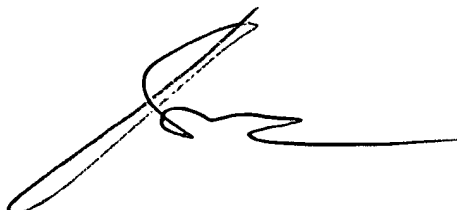
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV  
6/22/06

A handwritten signature in black ink, appearing to be 'KIM HUYNH', written over a horizontal line.

**KIM HUYNH**  
**SUPERVISORY PATENT EXAMINER**

6/27/06